Listing and Amendments to the Claims

This listing of claims will replace the claims that were published in the PCT Application:

1. (currently amended) An image display screen including:

- light emitters ~~(4)~~ distributed in rows of light emitters and columns of light emitters to form an array of light emitters,
- means ~~(2, 6, 8, 10, 12; 40, 42, 44)~~ for controlling the emissions of the light emitters of the array including:
  - a) a first circuit ~~(6, 14, 16, 18)~~ for addressing a light emitter ~~(4)~~, associated with each light emitter of the array to control the current flowing through it, said circuit ~~(6)~~ including:
    - a first current modulator ~~(14)~~ intended to power said light emitter ~~(4)~~, said first modulator ~~(14)~~ including a gate electrode and two current-carrying electrodes,
    - a first storage capacitor ~~(16)~~ intended to set a potential at the gate electrode of the first current modulator ~~(14)~~,
  - b) for each light emitter ~~(4)~~, at least a second circuit ~~(12, 34, 36, 38)~~ for addressing a light emitter, said first ~~(6)~~ and said second ~~(12)~~ addressing circuits being associated in parallel with the same light emitter ~~(4)~~, said second circuit ~~(12)~~ including:
    - a second current modulator ~~(34)~~ for said light emitter ~~(4)~~ including a gate electrode and two current-carrying electrodes,
    - a second storage capacitor ~~(36)~~ intended to store a potential at the gate electrode of the second current modulator ~~(34)~~;
  - c) addressing control means ~~(8, 11, 20, 22; 42, 46, 48, 50, 56)~~ intended to apply an addressing voltage ~~(V_D; D_{D1}, V_{D2})~~ at said first storage capacitor ~~(16)~~ and at said second storage capacitor ~~(16)~~, said addressing voltage representing an image datum, and being intended to activate either the first ~~(6)~~ or the second ~~(12)~~ addressing circuits in order to supply current to the light emitter ~~(4)~~ according to said image datum,

~~characterized in that~~ wherein the addressing control means ~~(8, 11, 20, 22; 42, 46, 48, 50, 56)~~ are intended to set a bias voltage ~~(V_p)~~ either at said first current modulator ~~(14)~~ or at said second current modulator ~~(34)~~, said bias voltage having an opposite polarity to the polarity of said addressing voltage.

2. (currently amended) The display screen as claimed in claim 1, ~~characterized in that~~ wherein the addressing control means ~~(8, 11, 20, 22; 42, 46, 48, 50, 56)~~ are intended to apply to said first current modulator ~~(14)~~ first the addressing voltage ~~(V_D; D_{D1}, V_{D2})~~ to start a phase ~~(B, C, D; G, H)~~ for activating the first addressing circuit ~~(6)~~, then the bias voltage ~~(V_p)~~ to start a phase ~~(E, F; I, J)~~ for biasing the first addressing circuit ~~(6)~~.

3. (currently amended) The display screen as claimed in claim 2, ~~characterized in that~~ wherein the addressing control means ~~(8, 11, 20, 22; 42, 46, 48, 50, 56)~~ are intended to apply to said second current modulator ~~(34)~~ first the addressing voltage ~~(V_D; D_{D1}, V_{D2})~~ to start a phase ~~(E, F; I, J)~~ for activating the second addressing circuit ~~(12)~~, then the bias voltage ~~(V_p)~~ to start a phase ~~(B, C, D; G, H)~~ for biasing the second addressing circuit ~~(12), in that~~ , wherein the phase for activating the first addressing circuit ~~(6)~~ is synchronous with the phase for biasing the second addressing circuit ~~(12)~~, and in that the phase for activating the second addressing circuit ~~(12)~~ is synchronous with the phase for biasing the first addressing circuit ~~(6)~~.

4. (currently amended) The display screen as claimed in ~~any one of the preceding claims, characterized in that~~ claim 1, wherein the control means include selection control means ~~(10, 11, 24, 26, 28; 44, 52, 54, 56)~~ including:

- for each first addressing circuit ~~(6)~~ for a light emitter, a first selection switch ~~(18)~~ intended to drive the transmission of said addressing voltage ~~(V_D; V_{D1}, V_{D2})~~ or of said bias voltage, as a function of a selection voltage ~~(V_{S1}, V_{S2}; V_S)~~, to said first storage capacitor ~~(16)~~ and said gate of said first current modulator ~~(14)~~ in order to select said light emitter ~~(4)~~;
- for each second addressing circuit ~~(12)~~ for the same light emitter, a second selection switch ~~(38)~~ intended to drive the transmission of said addressing voltage ~~(V_D; V_{D1}, V_{D2})~~ or of said bias voltage, as a function of said selection

voltage ~~(V_{S1}; V_{S2}; V_S)~~, to said second storage capacitor ~~(36)~~ and said gate of said second current modulator ~~(34)~~ in order to select said light emitter ~~(4)~~; and

- means ~~(11, 24, 26, 28; 52, 54, 56)~~ for driving the first ~~(18)~~ and second ~~(38)~~ selection switches.

5. (currently amended) The display screen as claimed in claim 4, ~~characterized in that~~ wherein the driving means ~~(11, 24, 26, 28; 52, 54, 56)~~ additionally include:

- for each row of light emitters, a first ~~(24)~~ and a second ~~(26)~~ selection electrode connected respectively to the first ~~(18)~~ and to the second ~~(38)~~ selection switches in order to control them; and
- a selection driving unit ~~(28)~~ intended to transmit, alternately, first said selection voltage ~~(V_{S1})~~ to said first selection electrode ~~(24)~~, then said selection voltage ~~(V_{S2})~~ to said second selection electrode ~~(26)~~.

6. (currently amended) The display screen as claimed in claim 5, ~~characterized in that~~ wherein the addressing control means ~~(8, 20, 22; 42, 46, 48, 50)~~ include:

- an addressing electrode ~~(20)~~ for each column of light emitters, the first ~~(18)~~ and the second ~~(38)~~ selection switches being connected to said addressing electrode ~~(20)~~; and
- an addressing driving unit ~~(22)~~ intended to send, alternately, said addressing voltage ~~(V_D)~~ and said bias voltage ~~(V_p)~~ to said addressing electrode ~~(20)~~.

7. (currently amended) The display screen as claimed in claim 4, ~~characterized in that~~ wherein the driving means ~~(11, 24, 26, 28; 52, 54, 56)~~ additionally include:

- a selection electrode ~~(52)~~ for each row of light emitters, the first ~~(18)~~ and second ~~(38)~~ selection switches being connected to said selection electrode ~~(52)~~ in order to control them; and
- a selection driving unit ~~(54)~~ intended to send said selection voltage ~~(V_S)~~ concomitantly to the first ~~(18)~~ and second ~~(38)~~ selection switches.

8. (currently amended)The display screen as claimed in claim 7, ~~characterized in that~~ wherein the addressing control means ~~(8, 20, 22; 42, 46, 48, 50)~~ include:

- for each column of light emitters, a first ~~(48)~~ and a second ~~(50)~~ addressing electrode connected respectively to the first (18) and to the second ~~(38)~~ selection switches; and
- an addressing driving unit ~~(46)~~ intended to send concomitantly on the first addressing electrode ~~(48)~~ and on the second addressing electrode ~~(50)~~ either said addressing voltage ~~(V_{D1})~~ or said bias voltage ~~(V_p)~~.

9. (currently amended) An addressing method for an image display screen including light emitters ~~(4)~~, a first ~~(6)~~ and a second ~~(12)~~ addressing circuit, the first addressing circuit ~~(6)~~ including a first current modulator ~~(14)~~ connected to a light emitter ~~(4)~~, a first storage capacitor ~~(16)~~ intended to store a potential at the gate of the first current modulator ~~(14)~~, said second addressing circuit ~~(12)~~ including a second current modulator ~~(34)~~ connected to said light emitter ~~(4)~~, a second storage capacitor ~~(36)~~ intended to store a potential at the gate of the second current modulator ~~(14)~~; each modulator ~~(14, 34)~~ including in particular a gate electrode and a source electrode; each modulator having a current pass through it when a voltage greater than a trigger threshold voltage is applied between its gate electrode and its source electrode,

~~characterized in that~~ wherein the method includes, for the driving of each light emitter ~~(4)~~:

- a phase ~~(B, C, D; G, H)~~ for activating the first addressing circuit ~~(6)~~ in order to supply current to the light emitter ~~(4)~~;
- a phase ~~(B, C, D; G, H)~~ for biasing the second addressing circuit ~~(12)~~ in order to shift the trigger threshold voltage of the second modulator ~~(34)~~;
- a phase ~~(E, F; I, J)~~ for activating the second addressing circuit ~~(12)~~ in order to supply current to the light emitter ~~(4)~~; and
- a phase ~~(E, F; I, J)~~ for biasing the first addressing circuit ~~(6)~~ in order to shift the trigger threshold voltage of the first modulator ~~(34)~~,

and ~~in that~~ wherein the phase for activating the first addressing circuit ~~(6)~~ is concomitant with the phase for biasing the second addressing circuit ~~(12)~~, and the

phase for activating the second addressing circuit ~~(12)~~ is concomitant with the phase for biasing the first addressing circuit ~~(6)~~.

10. (currently amended) The addressing method as claimed in claim 9, ~~characterized in that~~ wherein one or more phases for activating the first addressing circuit ~~(6)~~ are followed by at least one phase for biasing the first addressing circuit ~~(6)~~, and one or more phases for activating the second addressing circuit ~~(12)~~ are followed by at least one phase for biasing the second addressing circuit ~~(12)~~.

11. (currently amended) The addressing method as claimed in claim 9 ~~or 10, characterized in that~~ , wherein it includes:

- an addressing programming step ~~(B; G)~~ for said first storage capacitor by applying an addressing voltage ~~(V_D; V_{D1}, V_{D2})~~ representing an image datum to said capacitor;
- a bias programming step ~~(D; I)~~ for said first current modulator ~~(14)~~ by applying a bias voltage ~~(V_p)~~ to said modulator, said bias voltage having an opposite polarity to the polarity of the potential stored by the first storage capacitor ~~(16)~~;
- a bias programming step ~~(A; G)~~ for said second current modulator ~~(34)~~ by applying said bias voltage ~~(V_p)~~ to said modulator; and
- an addressing programming step ~~(E; I)~~ for said second storage capacitor ~~(36)~~ by applying said addressing voltage ~~(V_D; V_{D1}, V_{D2})~~ to said capacitor.

12. (currently amended) The addressing method as claimed in claim 11, ~~characterized in that~~ wherein the bias programming step ~~(D)~~ for said first current modulator ~~(14)~~ is followed by the addressing programming step ~~(E)~~ for the second storage capacitor ~~(36)~~, and alternately the bias programming step ~~(A)~~ for said second current modulator ~~(34)~~ is followed by the addressing programming step ~~(B)~~ for the first storage capacitor ~~(16)~~.

13. (currently amended) The addressing method as claimed in claim 11, ~~characterized in that~~ wherein said bias programming step ~~(G)~~ for said second current modulator ~~(34)~~ is concomitant with said addressing programming step ~~(G)~~ for said first storage capacitor ~~(16)~~, and said bias programming step ~~(I)~~ for said first current modulator ~~(14)~~ is concomitant with said addressing programming step ~~(I)~~ for said second storage capacitor ~~(36)~~.